Amendments to the Claims:

Listing of Claims:

Claim 1 (currently amended). A method of forming a gate structure comprising:

providing a substrate, and consecutively forming a gate oxide layer, a polysilicon layer, a silicide layer, and a cap layer onto the substrate;

patterning etching a portion of the cap layer, and the silicide layer, and the polysilicon layer to form a first stacked gate structure;

removing a portion of the silicide layer exposed on sidewalls of the <u>first</u> stacked gate structure for forming a recess on the sidewalls of the <u>first</u> stacked gate structure;

filling a passivation layer into the recess to form a second stacked gate structure; and

removing the remaining polysilicon layer and the gate oxide layer outside the sidewalls of the stacked gate structure using the second stacked gate structure as a mask.

Claims 2-3 (cancelled)

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Claim 4 (currently amended) The method of claim 1 wherein forming the <u>first</u> stacked gate structure comprises:

forming a patterned silicon oxynitride layer; and

utilizing the patterned silicon oxynitride layer as a hard mask to remove the cap layer, the silicide layer, and a portion of the polysilicon layer not covered by the patterned silicon oxynitride layer.

Claim 5 (currently amended) The method of claim 4 further comprising a

step of removing the patterned polysilicon oxynitride layer after removing the polysilicon layer and the gate oxide layer.

Claim 6 (original) The method of claim 1 wherein the silicide layer comprises tungsten silicon.

Claim 7 (original) The method of claim 1 wherein the recess is formed by removing a portion of the silicide layer using an ammonium hydrogen peroxide mixture (APM) solution.

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Claim 8 (original) The method of claim 1 wherein the passivation layer comprises silicon nitride.

Claim 9 (original) The method of claim 1 wherein filling the passivation layer into the recess further comprises:

depositing a silicon nitride layer onto the polysilicon layer and filling the recess; and

performing an anisotropic etching process to remove the silicon nitride layer outside the recess.

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Claim 10 (currently amended) A method of forming a gate structure comprising:

forming a patterned mask layer on the cap layer;

providing a substrate, and consecutively forming a gate oxide layer, a polysilicon layer, a silicide layer, and a cap layer onto the substrate;

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patterning etching the cap layer, and the silicide layer, and a portion of the polysilicon layer, and stopping etching on the polysilicon layer to form a first stacked gate structure using the

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patterned mask layer as a mask;

removing a portion of the silicide layer exposed on sidewalls of the <u>first</u> stacked gate structure with an etching solution to form a recess;

depositing a passivation layer onto the polysilicon layer and filling the recess, and performing an anisotropic etching process to remove the passivation layer outside besides the passivation layer filed in the recess to form a second stacked gate structure;

removing the polysilicon layer and the gate oxide layer not eovered by the patterned mask layer using the second stacked gate structure as a mask; and

removing the patterned mask layer.

Claim 11 (original) The method of claim 10 wherein the patterned mask layer comprises silicon oxynitride.

Claim 12 (original) The method of claim 10 wherein the steps of forming the patterned mask layer comprises:

forming a silicon oxynitride layer on the cap layer;

coating a photoresist layer on the silicon oxynitride;

performing an exposure process and a development process by using a photo mask to form a photoresist pattern;

utilizing the photoresist pattern as a hard mask to remove the silicon oxynitride not covered by the photoresist pattern; and

removing the photoresist pattern.

Claim 13 (original) The method of claim 10 wherein the silicide layer comprises tungsten silicon.

Claim 14 (original) The method of claim 10 wherein the etching solution is an ammonium hydrogen peroxide mixture (APM) solution.

5 Claim 15 (original) The method of claim 10 wherein the passivation layer comprises silicon nitride.